

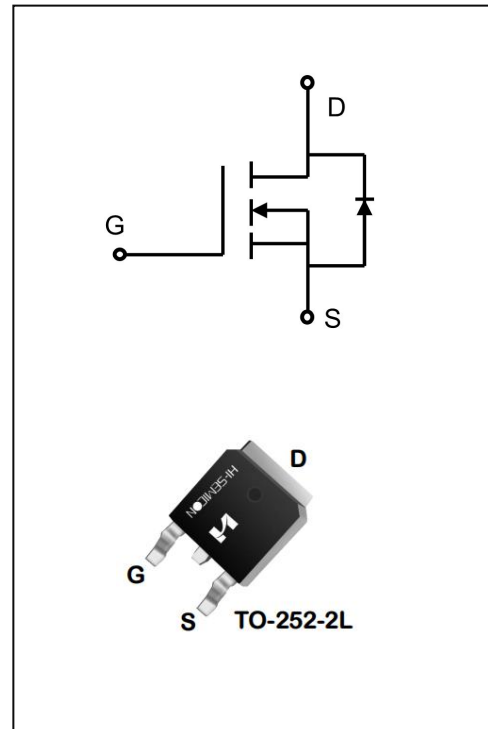
4A, 600V N-CHANNEL POWER MOSFET

GENERAL DESCRIPTION

These N-Channel enhancement mode power field effect transistors are produced using Hi-semicon's proprietary, planar stripe, VDMOS technology.

Features

- ◆ $V_{DS}(V)=600V$, $I_D=4A$
- ◆ $R_{DS(on)}$
 TYP: $2.4\Omega @ V_{GS}=10V$ $I_D=2A$
 MAX: 2.8Ω



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SFD4N60TS	TO-252-2L	SFD4N60TS	Pb free	Reel

ABSOLUTE MAXIMUM RATINGS ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Characteristics		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	± 30	V
Drain Current	$T_C = 25^{\circ}\text{C}$	I_D	4.0	A
	$T_C = 100^{\circ}\text{C}$		2.8	
Drain Current Pulsed (Note 1)		I_{DM}	16	A
Power Dissipation($T_C=25^{\circ}\text{C}$) -Derate above 25°C		P_D	56	W
			0.45	W/ $^{\circ}\text{C}$
Single Pulsed Avalanche Energy (Note 2)		E_{AS}	237	mJ
Operation Junction Temperature Range		T_J	$-55\sim+150$	$^{\circ}\text{C}$
Storage Temperature Range		T_{stg}	$-55\sim+150$	$^{\circ}\text{C}$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		TL	300	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	MAX	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.23	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	98	$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain -Source Breakdown Voltage	B _{VDSS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	100	nA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =30V, V _{DS} =0V	--	--	100	nA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =-30V, V _{DS} =0V	--	--	-100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	3.0	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =2.0A	--	2.4	2.8	Ω
Dynamic Characteristics						
Gate Resistance	R _g	V _{GS} =0V; f=1.0MHZ	--	4.2	--	Ω
Input Capacitance	C _{iSS}	V _{DS} =25V V _{GS} =0V f=1.0MHZ	--	616	--	pF
Output Capacitance	C _{oSS}		--	26	--	
Reverse Transfer Capacitance	C _{rSS}		--	5.1	--	
Switching Characteristics						
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V R _G =25Ω I _D =4A (Note 3.4)	--	14.8	--	ns
Turn-on Rise Time	t _r		--	26.4	--	

Turn-off Delay Time	$t_{d(off)}$	$V_{DD}=300V$ $R_G=25\Omega$	--	36.4	--	ns
Turn-off Fall Time	t_f	$I_D=4A$ (Note 3.4)	--	41.3	--	
Total Gate Charge	Q_g	$V_{DS}=480V$, $I_D=4A$ $V_{GS}=10V$ (Note 3.4)	--	13.2	--	nC
Gate-Source Charge	Q_{gs}		--	3.8	--	
Gate-Drain Charge	Q_{gd}		--	4.95	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	4	A
Pulsed Source Current	I_{SM}		--	--	16	
Diode Forward Voltage	V_{SD}	$I_S=4A$, $V_{GS}=0V$	--	1.0	1.4	V
Reverse Recovery Time	T_{rr}	$I_F=4A$, $V_R=300V$, $dI_F/dt=100A/\mu S$	--	32.8	--	ns
Reverse Recovery Charge	Q_{rr}		--	36.2	--	nC

1. Pulse width limited by maximum junction temperature
2. $L=10mH$, $I_{AS}=8.0A$, $V_{DD}=100V$, $V_G=10V$, $R_G=25\Omega$, starting $T_J=25^\circ C$
3. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature

Typical Performance Characteristics

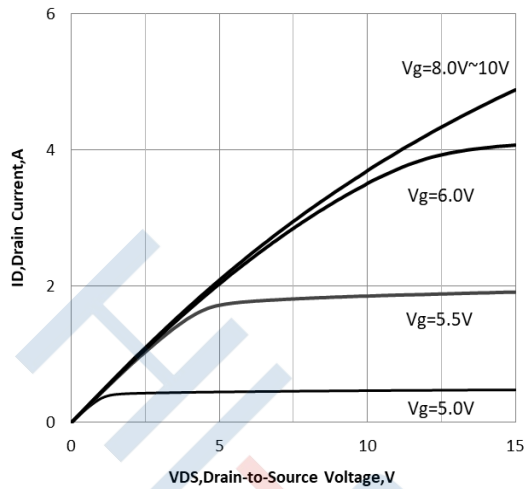


Figure.1 Typical Output Characteristics

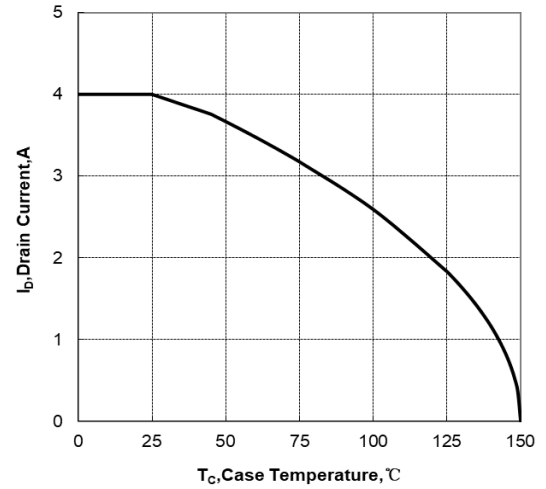


Figure.2 Maximum Continuous Drain Current vs Case Temperature

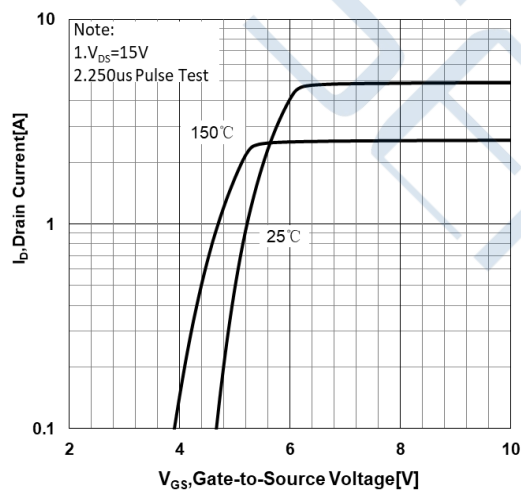


Figure.3 Typical Transfer Characteristics

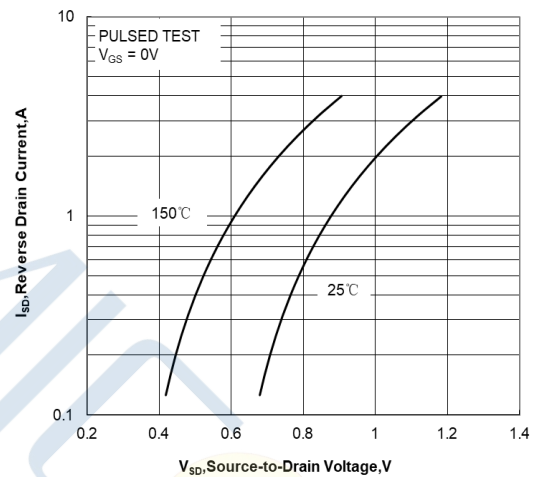


Figure.4 Typical Body Diode Transfer Characteristics

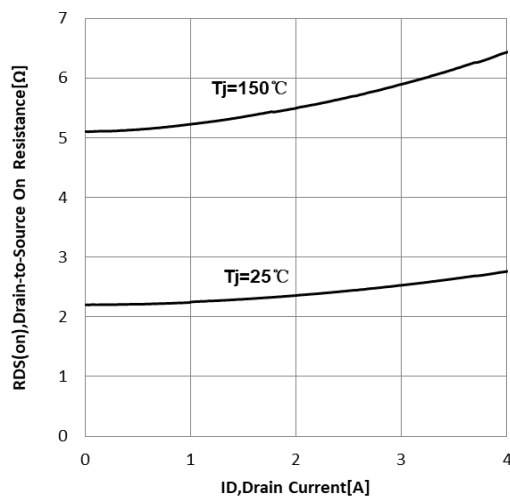


Figure.5 Typical Drain to Source ON Resistance vs Drain Current

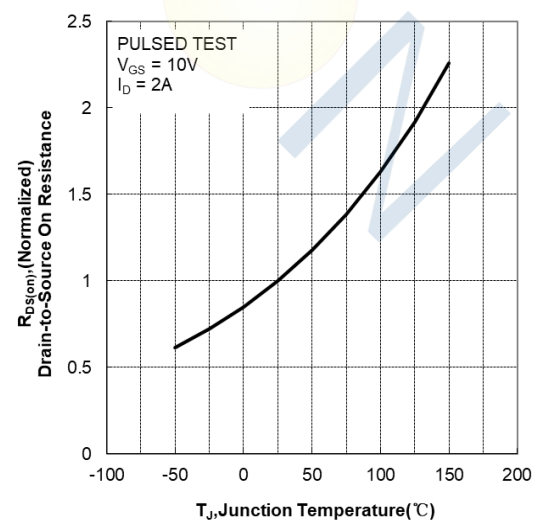


Figure.6 Typical Drain to Source on Resistance vs Junction Temperature

Typical Performance Characteristics

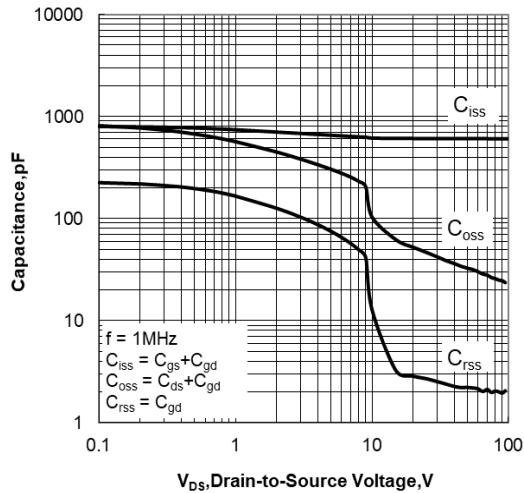


Figure.7 Typical Capacitance vs Drain to Source Voltage

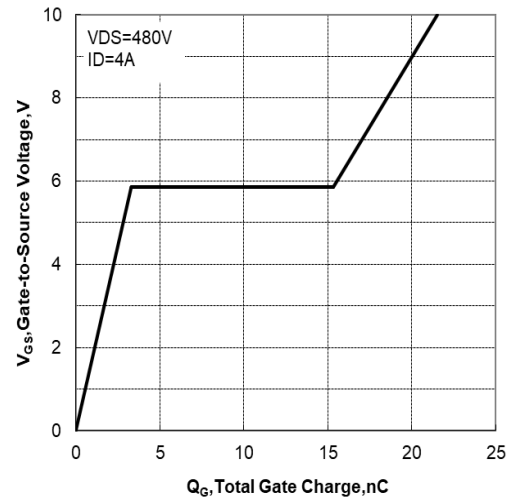


Figure.8 Typical Gate Charge vs Gate to Source Voltage

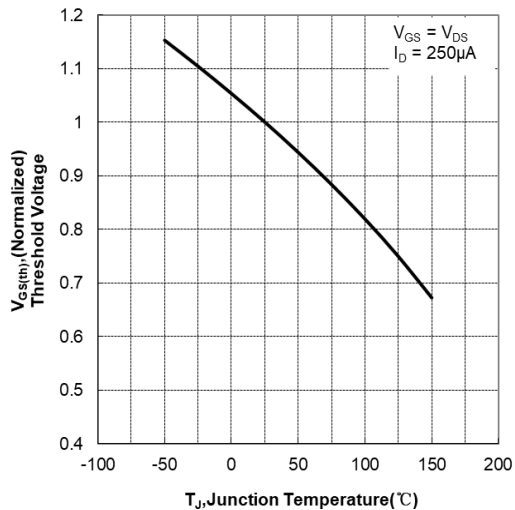


Figure.9 Typical Theshold Voltage vs Junction Temperature

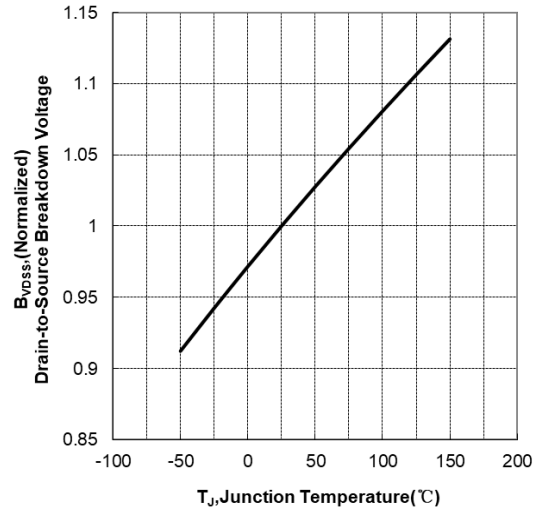


Figure 10 Typical Breakdown Voltage vs Junction Temperature

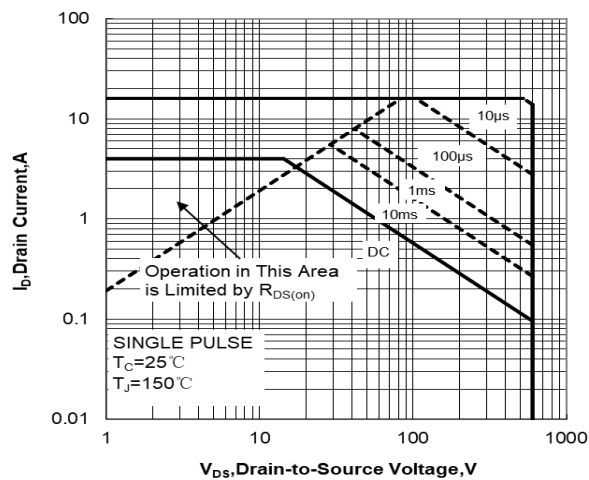
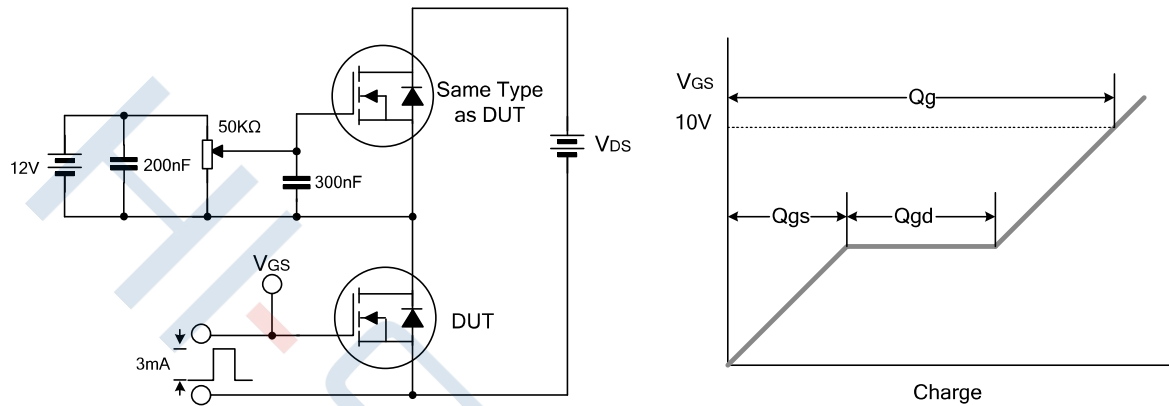


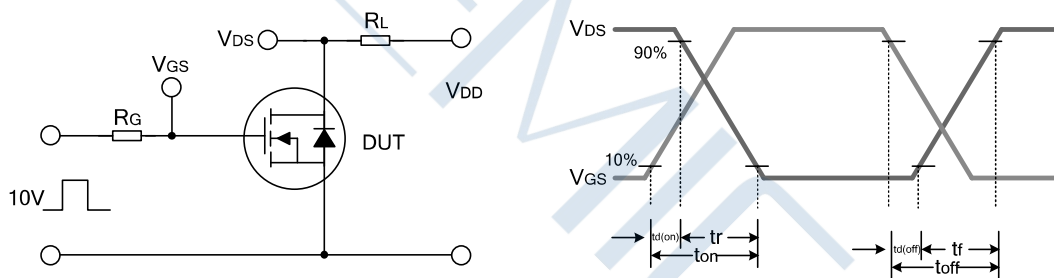
Figure.11 Maximum Forward Bias Safe Operating Area

Test Circuit

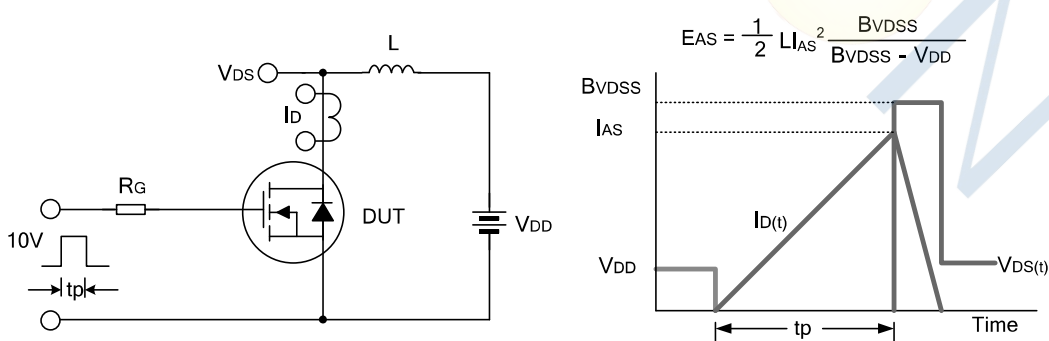
Gate Charge Test Circuit & Waveform



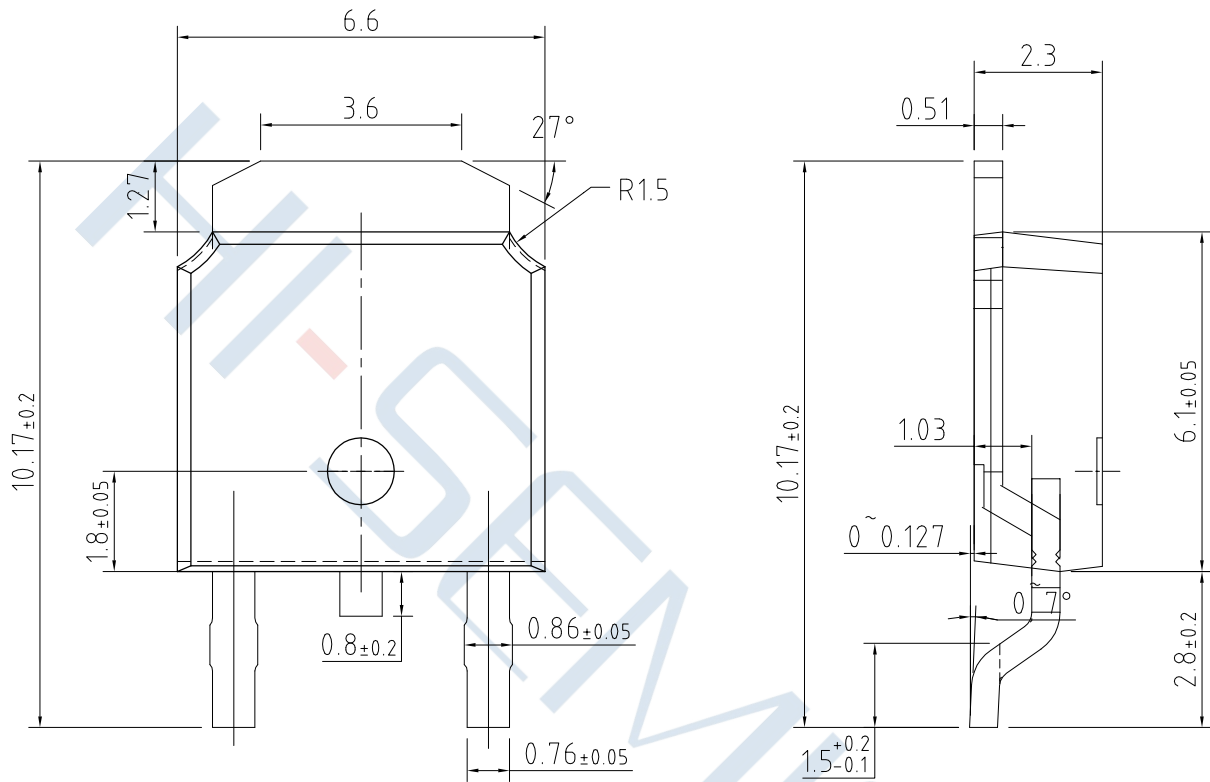
Resistive Switching Test Circuit & Waveform



Undamped Inductive Switching Test Circuit & Waveform



Package Dimensions of TO-252-2L



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